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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,929	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Brian L. Albertalli	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,8-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-15 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. The amendments to the claims have been entered. Claims 1-3, 8-15, 17, and 18 are currently amended, claims 4-7 and 16 are currently canceled, and new claims 19 and 20 have been added.

Response to Arguments

2. Applicant's arguments filed January 31, 2006 have been fully considered but they are not persuasive.

Before specifically addressing the Applicant's arguments, the terms "upper limit" and "lower limit" should be defined as used in the context of the present invention. As is illustrated by Fig. 5, an "upper limit" or "upper limit value" is a certain amplitude of positive excursion (i.e. a positive limit point amplitude above a central axis). A "lower limit" or "lower limit value" is a certain amplitude of negative excursion (i.e. a lower limit point amplitude below a central axis). This is consistent with the standard terminology as used in the art in reference to waveforms and limiters.

Claim 1

Regarding the rejection of claim 1 in view of Walley et al., the Applicant has alleged that "maximum excursion" as used by Walley et al. in the description of limit refers only to upper limit data, and thus Walley cannot anticipate "an upper limit data" as well as a "lower limit data" as now claimed (see page 12, lines 5-9 of Applicant's arguments).

This is not persuasive because, as is well known in the art, "conventional" clipping circuits as described by Walley et al. limit a signal according to a specific positive excursion *as well as* a specific negative excursion. The Applicant's assertion that "conventional clipping is understood to be for reducing loud signals, which are always high, not low" seems to ignore the fact that, when reducing loud signals, a conventional clipping circuit will limit the positive excursion as well as the negative excursion of the signal to the specified limits. A circuit which limits only "the upper limit data" is not a clipper, or limiter (as used interchangeably in the art), but is instead a *half wave rectifier*.

Furthermore, in response to the argument that Walleye et al. is "faulty" because in Fig. 2, the clip signal 23 goes to the D/A 18 and not clipping circuit 25, Walleye et al. clearly describe the clipping signal line 23 as being provided to clipping circuit 25 (column 2, lines 47-49). While the clipping signal line 23 in Fig. 2 may be in error, one of ordinary skill in the art would recognize that the description at column 2, lines 47-49 represents the correct embodiment of Walleye et al. Further, one of ordinary skill would recognize that it would be necessary for clipping signal line 23 to be connected to clipping circuit 25 rather than D/A 18 for the circuit to function correctly.

Regarding the rejection of claim 1 in view of Murata et al., the Applicant's arguments appear to be directed to new recitations in claim 19, not claim 1 (see page 12, lines 15-19). Accordingly, the Applicant's arguments with respect to the rejection of claim 1 in view of Murata et al. are considered moot.

Furthermore, Fig. 25 clearly illustrates an "upper limit data" and a "lower limit data" (clip value 114 as the positive excursion and clip value 114 as the negative excursion, respectively). The Applicant's argument that "the same value 104 [*sic, 114*] is applied to positive and negative excursions" does not apply to claim 1, as claim 1 does not require the upper limit data and lower limit data to be distinct values. That is, as illustrated by Fig. 25, upper limit data is output when pulse code modulation data is greater than upper limit data (positive excursion clip value 114) and lower limit data is output when pulse code modulation data is lower than lower limit data (negative excursion clip value 114).

Claims 2 and 3

Regarding the rejection of claims 2 and 3, since Murata et al. clearly discloses two data limits (i.e. clip value 114 as the positive excursion and clip value 114 as the negative excursion), the double application of a single element is clearly justified since the single comparator disclosed by Murata et al. (Fig. 26, 11a) compares the PCM code with an upper limit data (clip value 114 as the positive excursion) and compares the PCM code with a lower limit data (clip value 114 as the negative excursion).

Regarding claim 3, as discussed in the previous rejection, the circuit disclosed by Murata et al. is equivalent.

Other References

Applicant's arguments regarding Butcher and Wiatrowski fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Claims 8 and 17

Regarding the rejections of claims 8 and 17, the Applicant's allegation that average is not mentioned in the applied passage (page 13, final paragraph of Applicant's arguments) is not convincing because Butcher et al. clearly recite "the bias circuit is set to rapidly adjust the reference threshold in the limiter circuit to the average voltage of the incoming data signal" (emphasis added) in the previously recited passage (column 3, lines 1-8).

Furthermore, regarding the argument that Butcher et al. disclose an analog circuit (page 14, 1st paragraph of Applicant's arguments), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, one of ordinary skill would clearly recognize that, given the teaching of Butcher et al. to use an average of a signal as a limiter threshold, one would have to incorporate the required "calculating" circuit in Murata et al. to perform the averaging, as the system of Murata et al. is digitally implemented.

Regarding the argument that "the clipping circuit which clipped everything above the average value would have no output at all", the Applicant points to the dashed line in the middle of the signal of claim 25 alleging that this line represents the "average" (page 14, lines 7-12 of Applicant's arguments). Firstly, there is no indication in Murata et al. that this dashed line represents the "average" of the signal. This line simply represents the central axis of the signal.

Secondly, if the proposed combination of Murata et al. and Butcher et al. using a clipping circuit which clipped everything above the average value of a signal "would have no output at all", then claims 8 and 17 would appear to lack utility, as they perform the same function. That is claims 8 and 17 require a threshold value setting portion for calculating a limit data, wherein the threshold limit is determined by calculating an average of input PCM data and latching to said average value. This average value of the PCM, therefore, is used as the limit threshold above which everything is clipped. If the Applicant's maintain that such a system "would have no output at all", claims 8 and 17 may be rejected under 35 U.S.C. 101 for lacking utility.

Claim 10

Regarding claim 10, the Applicant has alleged Wiatrowski et al. teach counting only when a measurement is under a threshold, as opposed to counting when the measurement is over a threshold (see page 14, lines 20-24 of Applicant's arguments). However, the previously cited passage continues to recite: "Each time an attenuated signal is above the lower threshold, a value called symbol count is increased by 1"

(column 4, lines 59-63, emphasis added). Clearly, then Wiatrowski et al. teach counting when a measurement is over a threshold. Furthermore, the argument that the counter is simply reset when the count reaches 7 is not persuasive because Wiatrowski et al. teach when the symbol count reaches 7, the lower limit is increased (column 4, lines 63-65). The increase of the threshold would require a "voltage output" from the counter.

The Applicant's argument that the combination would not have been obvious because a single high value would not affect the threshold of Murata et al. (page 15, 2nd paragraph) is not persuasive because Murata et al., teach using a variable threshold (Fig. 29 and column 26, line 66 to column 27, line 6) which uses a maximum value as the clip value (threshold). A single high value during the max value detecting period (see Fig. 29) would set the threshold to that value, and thus cause the clip processor to allow overly high signals through during the clip period. Modifying Murata et al. by using the counting method disclosed by Wiatrowski et al. would mitigate this problem.

3. Therefore, for the reasons given above, the rejections made in the previous Office Action are maintained.

4. Furthermore, with regard to the use of official notice in the rejections of claim 9, it is noted that the applicant has not made any attempt to traverse the assertion of official notice, therefore the well-known in the art statement is taken to be admitted prior art (see MPEP 2144.03)

Specification

5. The amendments to the specification overcome the objections made in the previous Office Action. The objections to the specification are withdrawn.

Claim Rejections - 35 USC § 112

6. The amendments to claims 4-6 and 13-18 overcome the rejections made under 35 U.S.C. 112, 2nd paragraph in the previous rejection. The rejections of claims 4-6 and 13-18 under 35 U.S.C. 112, 2nd paragraph are withdrawn.

7. However, claim 10 is currently rejected under 35 U.S.C. 112, 2nd paragraph because claim 10 recites the limitation "the selected data" in line 9 of page 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Walley et al. (U.S. Patent 5,896,576).

In regard to claim 1, Walley et al. disclose an apparatus for decoding encoded voice data (Fig. 1) comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (modem 13, column 2, lines 21-30);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (ADPCM decoder 15, column 2, lines 31-34);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (modem 13 provides an error flag indicator, column 2, lines 27-30); and

a limiter which outputs said pulse code modulation data when the pulse code modulation data is within a range from an upper limit data to a lower limit data, outputs the upper limit data when the pulse code modulation data is greater than the upper limit data, and outputs the lower limit data when the pulse code modulation data is lower than the lower limit data, in accordance with said detection result (clipping circuit 25 activates when an error is detected, column 2, lines 47-52 and lines 56-63; a conventional clipping circuit will limit the positive excursion as well as the negative excursion of the signal to the specified limits).

10. Claims 1-3 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Murata et al. (U.S. Patent 5,925,146).

In regard to claim 1, Murata et al. disclose an apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (Fig. 36, conventional ADPCM reception unit 2 removes carrier wave, column 1, lines 48-50);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (1c, column 1, lines 35-38);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (Fig. 38, conventional error detection circuit column 2, lines 12-25); and

a limiter (clipper) which outputs said pulse code modulation data when the pulse code modulation data is within a range from an upper limit data to a lower limit data, outputs the upper limit data when the pulse code modulation data is greater than the upper limit data, and outputs the lower limit data when the pulse code modulation data is lower than the lower limit data, in accordance with said detection result (Fig. 24, clip processor 11 limits the amplitude of the PCM code to the clip value signal 114, column 24, lines 49-65; Fig. 25, the clip value signal 114 includes positive excursion value and a negative excursion value).

In regard to claim 2, Murata et al. disclose:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result (Fig. 26, comparator 11a

compares the positive amplitude of input PCM data with the clip value 114, column 26, lines 7-19);

a second comparator which compares said pulse code modulation data and said lower limit data and which outputs a second comparison result (comparator 11a compares the negative amplitude of the PCM data with the clip value 114, column 26, lines 7-19); and

a first output portion which outputs said pulse code modulation data, said upper limit data or said lower limit data in accordance with said detection result and said first and second comparison results (when the PCM amplitude is greater than the clip value, the clip value is output with the appropriate sign, i.e. positive or negative; when the PCM amplitude is less than the clip value, the PCM data is output, column 26, lines 7-19).

In regard to claim 3, Murata et al. disclose said first output portion comprises:

a first logic circuit which outputs a first logic circuit result having a first voltage level when both a voltage level of said first comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second logic circuit which outputs a second logic circuit result having said first voltage level when both a voltage level of said second comparison result and of said detection result are said first voltage level (similarly, the negative comparison results are only activated in response to the error detection information 102, and thus the circuits are equivalent, column 25, lines 46-62); and

a selector which selects said upper limit data when said first logic circuit result having said first voltage level is input, selects said lower limit data when said second logic circuit result having said first voltage level is input, or selects said pulse code modulation data when said first and second logic circuit results each not having said first voltage level is input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62).

In regard to claim 19, Murata et al. disclose the upper limit data is a largest amplitude value of a voice signal at which the reproduced voice signal does not have noise (Fig. 29, the maximum positive excursion detected during max value detecting period, column 26, line 66 to column 27, line 6), and the lower limit value is the smallest amplitude value of a voice signal at which the reproduced signal does not have noise (the maximum negative excursion detected during max value detecting period, column 26, line 66 to column 27, line 6).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 8, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al., in view of Butcher et al. (U.S. Patent 4,575,863).

In regard to claim 8, Murata et al. disclose an apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (Fig. 36, conventional ADPCM reception unit 2 removes carrier wave, column 1, lines 48-50);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (1c, column 1, lines 35-38);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (Fig. 38, conventional error detection circuit column 2, lines 12-25); and

a first threshold value setting portion which calculates a limit data based on said pulse code modulation data and which outputs said limit data (Fig. 28, maximum value

detector 12 sets the clip value signal 114, column 26, line 66 to column 27, line 6), wherein the threshold value setting portion comprises:

a latch portion which latches a maximal value and which outputs said maximal value based on a voltage level of a control signal (Fig. 30, when an error is detected register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18); and

a limiter (clipper) which outputs either said pulse code modulation data or a limit data in accordance with said detection result (Fig. 24, clip processor 11 limits the amplitude of the PCM code to the clip value signal 114, column 24, lines 49-65).

Murata et al. do not disclose determining the average value of numerical value data of said pulse code modulation data.

Butcher et al. disclose a limiter circuit that uses an average of the incoming signal to set the threshold of the limiter (column 3, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to use an average value calculation to set the threshold, instead of a maximal value, so that a large peak in the incoming PCM signal would not set the threshold of the limiter so high as to allow large bursts of noise.

In regard to claim 17, Murata et al. disclose an apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (Fig. 36, conventional ADPCM reception unit 2 removes carrier wave, column 1, lines 48-50);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (1c, column 1, lines 35-38);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (Fig. 38, conventional error detection circuit column 2, lines 12-25); and

a threshold value setting portion which calculates a limit data based on said pulse code modulation data produced at a term and which outputs said limit data, wherein said term is a term that a transmission error is not present in said encoded voice signal (Fig. 28, maximum value detector 12 sets the clip value signal 114 during a non-error detected term, column 26, line 66 to column 27, line 6), wherein the threshold value setting portion comprises:

an output portion which stores a maximal value based on the voltage levels of a control signal and said detection results and which outputs a stored maximal value as said limit data (Fig. 30, when an error is detected register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18); and

a limiter (clipper) which outputs either said pulse code modulation data or a limit data in accordance with said detection result (Fig. 24, clip processor 11 limits the amplitude of the PCM code to the clip value signal 114, column 24, lines 49-65).

Murata et al. do not disclose determining the average value of numerical value data of said pulse code modulation data.

Butcher et al. disclose a limiter circuit that uses an average of the incoming signal to set the threshold of the limiter (column 3, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to use an average value calculation to set the threshold, instead of a maximal value, so that a large peak in the incoming PCM signal would not set the threshold of the limiter so high as to allow large bursts of noise.

In regard to claim 18, the limitation Murata et al. disclose said third output portion comprises:

a logic circuit which outputs a logic circuit result having said first voltage level when a voltage level of said control signal is said first voltage level and when a voltage level of said detection result is a second voltage level (Fig. 30, when an error is detected register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the latch to go to the limiter in the event of an error detection; since the maximum value of Murata et al. are only held in response to the error detection information 102, the circuits are equivalent) and

a second latch port in which stores said average value based on a voltage level of said logic circuit result and which outputs a stored average value (when an error is detected

register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18).

13. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al., in view of Butcher et al., and further in view of Applicant's Admitted Prior Art (see Response to Arguments section, above).

Neither Murata et al. nor Butcher et al. disclose the details as to how the average calculating portion calculates an average.

The Applicant's Admitted Prior Art discloses that it is notoriously well known in the art that an average of a signal can be found by using an average calculating portion comprising:

an accumulator which executes an addition of said numerical value data of said pulse code modulation data and a stored value, which replaces said stored value with an addition result and outputs said addition result; and

a multiple portion which executes a multiple operation of said addition result and a coefficient.

It would have been obvious to one of ordinary skill in the art at the time of invention to further modify the combination of Murata et al. and Butcher et al. so as to perform the averaging operation with an accumulator and a multiple portion, since adding the numerical data of any signal and multiplying by a coefficient (i.e. dividing by a constant) is the typical method for calculating the average of a signal.

14. Claims 10-15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al., in view of Wiatrowski et al. (U.S. Patent 5,521,941).

In regard to claim 10, Murata et al. disclose an apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (Fig. 36, conventional ADPCM reception unit 2 removes carrier wave, column 1, lines 48-50);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (1c, column 1, lines 35-38);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (Fig. 38, conventional error detection circuit column 2, lines 12-25); and

a first threshold value setting portion which calculates a limit data based on said pulse code modulation data and which outputs said limit data (Fig. 28, maximum value detector 12 sets the clip value signal 114, column 26, line 66 to column 27, line 6); and

a limiter (clipper) which outputs either said pulse code modulation data or a limit data in accordance with said detection result (Fig. 24, clip processor 11 limits the amplitude of the PCM code to the clip value signal 114, column 24, lines 49-65).

Murata et al. do not disclose:

a counter which counts the number of times that said pulse code modulation data is over said limit data and which outputs a count result having a first voltage level when said count result is over a predetermined value.

Wiatrowski et al. disclose system for setting a threshold value (limit) of a received signal that comprises:

a counter which counts the number of times that pulse code modulation data is over said limit data (symbol count) and which outputs a count result having a first voltage level when said count result is over a predetermined value (when a symbol is measured to be above a limit threshold, the symbol count is increased by one, until the symbol count reaches 7, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to include a counter to count the number of times pulse code modulation data is over said limit data, and output data in accordance with that result so that a single high value pulse code modulation data value would not set the threshold too high so as to allow bursts of noise.

In regard to claim 11, Murata et al. disclose said limit data has an upper limit data (Fig. 25, upper clip value 114) and a lower limit data (lower clip value 114); and wherein said limiter comprises:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result (Fig. 26, comparator 11a

compares the positive amplitude of input PCM data with the clip value 114, column 26, lines 7-19);

a second comparator which compares said pulse code modulation data and said lower limit data and which outputs a second comparison result (comparator 11a compares the negative amplitude of the PCM data with the clip value 114, column 26, lines 7-19).

Murata et al. do not disclose a fourth output portion which does not output said pulse code modulation data when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the pulse code modulation data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 12, Murata et al. disclose a first logic circuit which outputs a first logic circuit result having a first voltage level when both a voltage level of said first comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate

acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second logic circuit which outputs a second logic circuit result having said first voltage level when both a voltage level of said second comparison result and of said detection result are said first voltage level (similarly, the negative comparison results are only activated in response to the error detection information 102, and thus the circuits are equivalent, column 25, lines 46-62); and

a first selector which selects said upper limit data when said first logic circuit result having said first voltage level is input, said lower limit data when said second logic circuit result having said first voltage level is input or said pulse code modulation data when said first and second logic circuit results each not having said first voltage level is input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62).

Murata et al. do not disclose a fourth output portion which does not output said pulse code modulation data when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the pulse code modulation data when said

count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 13, Murata et al. disclose a format of said limit data is the absolute value (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, therefore, the clip value must be an absolute value, column 26, lines 17-19); and wherein said limiter portion comprises:

a third comparator which compares a numerical value data of said pulse code modulation data and said limit data and which outputs a third comparison result (Fig. 26, comparator 11a, column 26, lines 7-19); and

Murata et al. do not disclose a fifth output portion which does not output said pulse code modulation data or said limit data when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the pulse code modulation data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 14, Murata et al. discloses said fifth output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second selector which selects said limit data when said third logic circuit result having said first voltage level is input or said numerical value data when said third logic circuit result having said first voltage level is not input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62); and

a first combiner which combines a code data (sign of the input PCM code) of said pulse code modulation data and said data selected by said second selector and which outputs a combined data (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, column 26, lines 17-19).

Murata does not disclose a controller which does not output said combined data output by said first count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the combined data (PCM data with a sign bit) data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 15, Murata et al. disclose said second output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second combiner which combines a code data of said pulse code modulation data and said limit data and which outputs a combined limit data (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, column 26, lines 17-19).

Murata et al. do not disclose a third selector which does not select said combined limit data and said pulse code modulation when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the combined data (PCM data with a sign bit) and said pulse code modulation data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 20, Murata et al. do not disclose the upper limit value and lower limit value are set individually and freely.

Wiatrowski et al. disclose an upper limit value and a lower limit value that is set independently and freely (by upper threshold adjustment circuit in Fig. 3A and lower threshold adjustment circuit in 3B, column 3, lines 11-12 and lines 63-66; each threshold generator keeps a separate count, column 4, lines 58-59).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to allow the upper threshold and lower threshold to be set individually and freely, in order to compensate for any bias offsets in the received signal (by adjusting the upper limit and lower limit accordingly).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. IEEE (*IEEE 100*) discloses standard limiter circuits prevent output from exceeding a given value independent of sign (i.e. for both positive excursion and negative excursion).

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Albertalli whose telephone number is (571) 272-7616. The examiner can normally be reached on Mon - Fri, 8:00 AM - 5:30 PM, every second Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (571) 272-7843. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BLA 4/6/06

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